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DATE: January 22, 2004

PTO IDENTIFIER: **Application Number** 09/588,617-Conf. #1077
Patent Number

Inventor: Claude L. Bertin et al.

MESSAGE TO: DIRECTOR TC 2800 (MS PETITIONS)

SUBJECT: Petition to Withdraw Holding of Abandonment by Examiner

FAX NUMBER: (703) 872-9306

FROM: CONNOLLY BOVE LODGE & HUTZ LLP
Larry J. Hume

PHONE: (202) 331-7111

Attorney Dkt. #: 21806-00083-US

PAGES (Including Cover Sheet): 32

CONTENTS:

Petition to Withdraw Holding of Abandonment by Examiner under 37 CFR §1.181 (4 pages);
Official Action mailed 10/9/03 (7 pages);
Amendment/Response Filed 1/9/04 (with facsimile confirmation receipt) (15 pages);
Notice of Abandonment mailed 1/14/04 (2 pages);
USPTO PAIR Status Pages indicating application is "lost" (2 pages); and
Certificate of Transmission (1 page).

NO FEE IS DUE.

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PAGE 1/32 * RCVD AT 1/22/2004 3:20:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:2022936229 * DURATION (mm-ss):08-12

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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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on January 22, 2004
Date

Larry J. Hume
Signature

Larry J. Hume
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Docket No.: 21806-00083-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Claude L. Bertin, et al.

Conf. No. 1077

Application No.: 09/588,617

Art Unit: 2829

Filed: June 6, 2000

Examiner: T. Nguyen

For: CARRIER FOR TEST, BURN-IN, AND FIRST LEVEL PACKAGING

PETITION TO WITHDRAW HOLDING OF ABANDONMENT BY EXAMINER PURSUANT TO 37 CFR 1.181(A)

MS PETITION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 22, 2004

Dear Sir:

Petitioner hereby petitions the Commissioner to withdraw the holding of abandonment in the Notification of Abandonment mailed on January 14, 2004. The Notification incorrectly stated that the Applicant failed to provide a timely reply to the Office letter mailed on April 22, 2003.

NO FEES ARE BELIEVED TO BE DUE WITH THIS PETITION.

Statement of the Relevant Facts

To the undersigned's knowledge and belief, and after making reasonable inquiry into the circumstances surrounding this application, a statement of the relevant facts with respect to this petition is provided below:

Application No.: 09/588,617 Docket No.: 21806-00083-US

(1) The current Assignee (IBM) received a telephone call from the Examiner on or about September 23, 2004, inquiring about a potential abandonment of this application. Assignee reportedly indicated to the Examiner that the application was not intended to be abandoned.

(2) Assignee's representative requested that the undersigned attorney with responsibility for prosecuting the application investigate the status of the case, and to ensure that the application was not allowed to go abandoned.

(3) The undersigned attorney contacted Supervisory Examiner Kamand Cuneo, on or about October 7, 2003, to inquire about the status of the case. Examiner Cuneo located the file, and determined that the purported Office action of April 22, 2003, which provided the basis for this Holding of Abandonment, had not been mailed to the undersigned or assignee.

(4) Subsequent to Examiner Cuneo's determination in (3) above, the mailing date of the Office Action was reset to October 9, 2003 (Paper No. 9), and the shortened statutory period for response was extended until January 9, 2004. A copy of this Office Action is provided as an attachment to this Petition.

(5) On January 9, 2004, the undersigned attorney prepared and timely filed a Amendment and Response to the Office Action of October 9, 2004. This filing was made by facsimile transmission to the USPTO centralized facsimile number, (703) 872-9306. A copy of this Amendment and Response is provided as an attachment to this Petition, along with a copy of the facsimile receipt from the USPTO RightFax System, showing receipt of the Amendment on the last day of the shortened statutory period, i.e., January 9, 2004, three (3) months from the mailing date of the Office Action of October 9, 2003.

(6) On January 14, 2004, a Notice of Abandonment in this application was mailed by the USPTO to Customer No. 30678 (Connolly Bove Lodge & Hutz LLP). The undersigned attorney received the Notice on January 15, 2004.

(7) The undersigned attorney did not receive any verbal communication from the Examiner during the period between October 9, 2003 and January 15, 2004.

(8) Subsequent to receipt of the Notice of Abandonment by the undersigned, voice messages were exchanged by the undersigned and Supervisory Examiner Cuneo on or about January 22, 2004. Examiner Cuneo indicated that the Abandonment was clearly in error due to USPTO mistake, but that a Petition by Applicant under 37 C.F.R. §1.181 would, unfortunately, be required to reactivate the application.

(9) Review of the PAIR Status page for this application, enclosed herewith, indicates that shortly after mailing the Notice of Abandonment, the file was marked "lost" by the USPTO on January 16, 2004.

(10) This Petition has been submitted upon the recommendation of Supervisory Examiner Kamand Cuneo, in Art Unit 2829, telephone no. (571) 272-1957.

Relief Sought by Applicant

Applicants respectfully request:

(A) That this Petition be treated on its merits, and that the holding of abandonment be withdrawn as if no abandonment had occurred.

(B) Applicants also request that this Petition be processed and approved without any fee, as the errors involved were clearly those of the USPTO.

(C) Applicants further request that the Amendment filed on January 9, 2004 be entered as timely filed, with no fee for any extension of time, and that examination of the application on the merits be continued without prejudice to Applicants, and without loss of any patent term that might result from successful prosecution and allowance of this application.

Application No.: 09/588,617 Docket No.: 21806-00083-US

No Fees are Believed to Be Due

Although no Petition fees are believed to be due in this matter because of clear USPTO error, if any fees are due, the Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 22-0185, under Order No. 21806-00083-US, from which the undersigned is authorized to draw.

Respectfully submitted,

By Larry J. Hume

Larry J. Hume
Registration No.: 44,163
CONNOLLY BOVE LODGE & HUTZ LLP
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Attorney for Applicant

Attachments: Official Action mailed 10/9/03
Amendment Filed 1/9/04 (with facsimile confirmation receipt)
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USPTO PAIR Status Page indicating application is "lost"

BAA/L3W

1/9/04

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,617	06/06/2000	Claude L. Bertin	BUR9-1999-0264-US1	1077

30678 7590 10/09/2003

CONNOLLY BOVE LODGE & HUTZ LLP
SUITE 800
1990 M STREET NW
WASHINGTON, DC 20036-3425

EXAMINER	
NGUYEN, TRUNG Q	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	09/588,617	BERTIN ET AL.	
	Examiner	Art Unit	
	Trung Q Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 June 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-29 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 1, the specification and drawings as original filed do not provide support for end use operation wherein "end use operation" has no characteristic where and how it is operated. In addition, How do the "end use operation" functions is not clear.

Claims 2-29 are rejected for being dependent on rejected claim 1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (U.S. 5,594,626), as best as the examiner is able to ascertain.

Regarding claims 1-3, 30-32, Restoker et al. disclose in Figures 6 and 14B and 15 a method for manufacturing and testing semiconductor components comprising plurality of semiconductor devices 1406 of Fig. 14B, a device carrier 600 of Fig. 6 having interconnect wiring therein (not shown), attaching semiconductor devices via chip or die [column 14, lines 30-37] to carrier 600; testing devices via wiring 614; dividing carrier 1408 of Fig. 14B into a plurality of components 1406 wherein each component 1406 contains at least one semiconductor device 600 wherein carrier 600 can be install to 1408 without separating device from carrier (Fig. 15).

Regarding claim 4, Restoker et al. disclose in Figures 6 and 14B carrier 600 comprises a printed circuit board 602.

Regarding claim 5, Restoker et al. disclose in Figures 6 and 14B semiconductor devices comprising plurality of leads 614 of Fig. 6 for external connection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker et al. (U.S. 5,594,626) in view of Kaneko et al. (U.S. 5,534,786).

Claims 13-18 and 21 add the limitation of running test independently of each of semiconductor devices, connecting leads in common and multi-chip assemblies. However, Rostoker Kaneko et al. disclose semiconductor devices (3) are organized in a plurality of groups on carrier (3 and 6 of Fig. 5); and testing groups of devices in parallel with a separate reader (9) for each group; a running semiconductor devices simultaneously independently of each other and single-in-line multi-chip modules assemblies (6, 7 and 8 of Fig. 5). Kaneko also discloses a step of mounting semiconductor component on a second carrier (7 and 8 of Fig. 5) wherein second carrier comprises a printed circuit board (column 4, lines 36-40).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to use the above steps as taught by Kaneko et al for the purpose of measuring the values of grating points and ensuring the positions of the each of the chip or die at the arbitrary positions with high accuracy and at a high rate.

Regarding claims 22-27, Kaneko et al. disclose the step of encapsulating semiconductor device and carrier (3 and 6 of Fig. 5) in an encapsulant (5); identifying and repairing defective semiconductor devices (column 3, 20-45 and column 5, lines 23-32).

Regarding claims 28-29, Kaneko et al. disclose the semiconductor devices are memory chips (column 4, line 48) and a step of testing functionality (column 5, lines 7-14).

Allowable Subject Matter

7. Claims 6-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: claim 6 recite, inter alia, "a built-in self-test engine (BIST), wherein, the BIST is a memory chip can provide patterns for burn-in and for final chip testing at speed, BIST engine may include complex patterns or perform redundancy calculations among other tasks." The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations.

Response to Arguments

8. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Nguyen whose telephone number is 703-305-

4925. The examiner can normally be reached on Monday through Friday, 8:30AM – 5:00PM. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached at (703) 308-1233.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

TN
April 10, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Auto-Reply Facsimile Transmission

TO: Fax Sender at 202 293 6229

Fax Information
Date Received: 1/9/2004 7:44:31 PM [Eastern Standard Time]
Total Pages: 14 (including cover page)

ADVISORY: This is an automatically generated return receipt confirmation of the facsimile transmission received by the Office. Please check to make sure that the number of pages listed as received in Total Pages above matches what was intended to be sent. Applicants are advised to retain this receipt in the unlikely event that proof of this facsimile transmission is necessary. Applicants are also advised to use the certificate of facsimile transmission procedures set forth in 37 CFR 1.8(a) and (b), 37 CFR 1.6(f). Trademark Applicants, also see the Trademark Manual of Examining Procedure (TMEP) section 306 et seq.

Received Cover Page ========>

Certificate of Transmission

I hereby certify that this correspondence, consisting of 14 pages, is being facsimile transmitted to the United States Patent and Trademark Office, Art Unit 2829, facsimile no. 703 872-9306, on January 9, 2004

Signature (Larry J. Hume)

Docket No.: 21806-00083-US
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Claude L. Bertin, et al.

Conf. No. 1077

Application No.: 09/588,617

Art Unit: 2829

Filed: June 6, 2000

Examiner: T. Nguyen

For: CARRIER FOR TEST, BURN-IN, AND FIRST LEVEL PACKAGING

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 9, 2004

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated October 9, 2003 (Paper No. 9), please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

No fees are due with this Amendment.

Certificate of Transmission

I hereby certify that this correspondence, consisting of 14 pages, is being facsimile transmitted to the United States Patent and Trademark Office, Art Unit 2829, facsimile no. 703 872-9306, on January 9, 2004.

Signature (Larry J. Hume)

Docket No.: 21806-00083-US
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Claude L. Bertin, et al.

Conf. No. 1077

Application No.: 09/588,617

Art Unit: 2829

Filed: June 6, 2000

Examiner: T. Nguyen

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MS Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 9, 2004

Dear Sir:

INTRODUCTORY COMMENTS

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Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

No fees are due with this amendment.

13349_DC

Application No.: 09/588,617 Docket No.: 21806-00083-US

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently amended) ~~The~~ A method for manufacturing and testing semiconductor components, the method comprising ~~the steps of~~:

providing a plurality of semiconductor devices;

providing a device carrier, said carrier having interconnect wiring therein sufficient for both operational testing and ~~end use operation~~packaging of said semiconductor devices;

attaching said semiconductor devices to said carrier;

testing said devices via said wiring; and

dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device.

2 (Original) The method according to claim 1, further comprising the step of installing one said component on a next level of assembly without separating said device from said carrier.

3. (Original) The method according to claim 1, further comprising the step of installing one said component in an information handling system without separating said device from said carrier.

4. (Original) The method according to claim 1, wherein said carrier comprises a

printed circuit board or a flex.

5. (Original) The method according to claim 1, wherein each of said semiconductor devices comprises a plurality of leads and wherein said carrier comprises contacts for external connection, the method further comprising the step of providing a lead reduction mechanism on said carrier, said lead reduction mechanism connected to said carrier contacts.

6. (Original) The method according to claim 5, wherein said lead reduction mechanism comprises a built-in self-test engine.

7. (Original) The method according to claim 6, wherein each semiconductor device comprises one said built-in self-test engine.

8. (Original) The method according to claim 7, wherein said built-in self-test engine includes less than ten external contacts for controlling said test engine, and wherein said semiconductor devices are connected in parallel to said external contacts for test or burn-in.

9. (Original) The method according to claim 7, wherein said semiconductor devices are organized in a plurality of groups on said carrier wherein BIST pads on said devices in each group are connected in parallel to separate external contacts.

10. (Original) The method according to claim 9, further comprising the step of burning-in or testing groups of devices in parallel with a separate BIST reader for each group.

11. (Original) The method according to claim 6, further comprising the step of testing or burning in said semiconductor devices using said built-in test engine.

12. (Original) The method according to claim 11, further comprising the step of separating said built-in self test engine from said carrier.

13. (Original) The method according to claim 1, wherein said testing step comprises running said semiconductor devices simultaneously and independently of each other.

14. (Original) The method according to claim 1, wherein said lead reduction mechanism comprises connecting like leads of said plurality of semiconductor devices in common.

15. (Original) The method according to claim 1, wherein the method comprises dividing said carrier into separate multi-chip final assemblies.

16. (Original) The method according to claim 15, wherein said multi-chip assemblies comprises single-in-line multi-chip modules or dual-in-line multi-chip modules.

17. (Original) The method according to claim 1, further comprising the step of mounting said semiconductor component on a second carrier.

18. (Original) The method according to claim 17, wherein said carrier comprises a flex, and wherein said second carrier comprises a printed circuit board, a second flex, a ceramic substrate, or a semiconductor substrate.

19. (Original) The method according to claim 18, wherein said flex comprises leads, said method further comprising separating adjacent leads from each other to facilitate connection to said second carrier.

20. (Original) The method according to claim 18, wherein a plurality of said components are connected to said second carrier to form an interconnected stack.

21. (Original) The method according to claim 1, wherein said carrier comprises connectors for connecting semiconductor devices on two sides of said carrier.

22. (Original) The method according to claim 1, further comprising the step of encapsulating said semiconductor devices and said carrier in an encapsulant.

23. (Original) The method according to claim 1, further comprising the step of identifying defective semiconductor devices.

24. (Original) The method according to claim 23, further comprising the step of invoking redundancy to repair said defective devices.

25. (Original) The method according to claim 23, further comprising the step of removing and replacing said defective semiconductor devices with replacement semiconductor devices.

26. (Original) The method according to claim 25, further comprising the step of repeating said testing, identifying, and removing and replacing until no defective semiconductor devices are identified.

27. (Original) The method according to claim 25, wherein said replacement semiconductor devices have passed testing and burning-in on another carrier so no further burning-in is required.

28. (Original) The method according to claim 1, wherein said semiconductor devices are memory chips, the method further comprising testing said memory chips at speed.

29. (Original) The method according to claim 1, wherein said testing comprises testing functionality, testing for sensitivities, or testing fuses.

30. (Currently amended) A semiconductor structure comprising:

a device carrier~~, said carrier having interconnect wiring therein sufficient for both testing and end use operation of said semiconductor devices~~; and

a plurality of semiconductor devices mounted to said device carrier,

said device carrier having interconnect wiring therein sufficient for both testing and

packaging of said semiconductor devices; ~~and~~

wherein said semiconductor devices on said carrier ~~may~~ are arranged to be tested and burned-in, ~~and~~

wherein said carrier ~~may~~ is arranged to be divided into a plurality of components, and

wherein said plurality of components ~~may be~~ are arranged so as to be suitably installed in an information handling system without separating said semiconductor devices from said device carrier.

31. (Original) The semiconductor structure of claim 30 wherein said carrier comprises contacts for external connection, said structure further comprising a lead reduction mechanism on said carrier, said lead reduction mechanism connected to said contacts of said carrier.

32. (Currently amended) A semiconductor structure comprising:

a stack of flex device carriers, at least one semiconductor device mounted to each said flex carrier; and

an interconnect substrate, wherein said flex device carriers are electrically connected to said interconnect substrate,

wherein said stack of flex device carriers, said at least one semiconductor device, and said interconnect substrate are interconnected and arranged in a manner suitable for both operational testing and packaging of the semiconductor structure.

Application No.: 09/588,617 Docket No.: 21806-00083-US

REMARKS

Claims 1-32 remain pending in this application. Claims 1, 30, and 32 are independent. Claims 1, 30, and 32 have been amended, and no claims have been canceled or added by this amendment.

Withdrawal of the rejection of claims 1-29 under 35 U.S.C. §112, first paragraph, for lack of written description, is requested. Applicants submit that a person with skill in the art would appreciate and understand the concept and context of "interconnect wiring...sufficient for both testing and end use operation of said semiconductor devices", as recited in original claim 1, particularly in light of the Specification at, for example, page 16, lines 21-24 and at page 19, lines 7-24.

However, to expedite prosecution of this application and passage to issue, independent claim 1 has been amended to recite "packaging" instead of "end use operation", thus rendering the §112 (¶1) rejection moot.

Anticipation Rejection

Withdrawal of the rejection of claims 1-32 under 35 U.S.C. §102(b) as being anticipated by Rostoker et al. (US 5,594,626).

Applicant notes that anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[2] To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in

[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim limitation may be ignored.[6]

Deficiencies of Rostoker et al.

The applied art does not disclose a method for manufacturing and testing semiconductor components, which includes, among other features, "...providing a device carrier...having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices...testing said devices via said wiring; and dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device, as recited in independent claim 1, as amended.

In addition, the applied art does not disclose a semiconductor structure which includes, among other features, "...a device carrier...having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices; wherein said semiconductor devices on said carrier are arranged to be tested and burned-in...and wherein said plurality of components are arranged so as to be suitably installed in an information handling system without separating said semiconductor devices from said device carrier", as recited in independent claim 30, as amended.

Finally, the applied art does not disclose a semiconductor structure which includes, among other features, "...a stack of flex device carriers, at least one semiconductor device mounted to each said flex carrier; and an interconnect substrate...wherein said stack of flex device carriers, said at least one semiconductor device, and said interconnect substrate are interconnected and arranged in a manner suitable for both operational testing and packaging of the semiconductor structure", as recited in independent claim 32, as amended.

Rostoker et al. is directed to a partially-molded PCB chip carrier package for non-square die shapes which have a high pin count. The non-square shape enables Rostoker et al., at least in part, to better accommodate high pin count chips, carriers, and associated leads. Applicants

[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).
[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).

submit that Rostoker et al. does not disclose or contemplate use of interconnect wiring in a device carrier sufficient for both operational testing and packaging.

Instead, Rostoker et al. FIG. 6 illustrates an embodiment arranged with a certain perimeter-to-area ratio of a greatly elongated rectangular die-receiving area which accommodates 15% more conductive lines than a similar prior art size (square) die-receiving area. Rostoker et al. FIG. 14B illustrates a plan view of a number of greatly elongated rectangular semiconductor packages (e.g., as shown in FIG. 6) on a printed circuit mother board. Rostoker et al. FIG. 15 illustrates a plan view of a leadframe element for a package adapted to triangular die and package shapes.

None of these Figures teach or suggest the limitations in independent claims 1, 30, or 32, particularly relating to use of interconnect wiring which is sufficient for both testing and packaging of semiconductor devices, as variously claimed, and as would be understood by a person having skill in the art, in light of the Specification.

Therefore, withdrawal of the rejection and allowance of independent claims 1, 30, and 32 are requested. Further, dependent claims 2-29, variously and ultimately depend upon allowable claim 1, and dependent claim 31 depends upon allowable claim 30. Allowance of these claims is also requested.

Unpatentability Rejection

Withdrawal of the rejection of claims 13-29 under 35 U.S.C. §103(a) as being unpatentable over Rostoker et al. in view of previously cited Kaneko et al. (US 5,354,786) is requested.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim

limitations.[7] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[8]

Not only does Kaneko et al. not make up for the previously identified deficiencies of Rostoker et al. at least with respect to independent claim 1, Applicants submit that proper motivation to combine the applied art in the manner suggested by the Examiner has not been established, because Kaneko et al. teaches away from at least one aspect of the claimed invention.

Rostoker et al. and Kaneko et al. do not Teach all Limitations

All the claim limitations must be taught or suggested by the prior art.[9] All words in a claim must be considered in judging the patentability of that claim against the prior art.[10]. When evaluating the scope of a claim, every limitation in the claim must be considered.[11] The evidentiary record fails to teach each limitation of the claimed invention.

Kaneko et al. does not teach or suggest, either alone or in combination, a method for manufacturing and testing semiconductor components, which includes, among other features, "...providing a device carrier...***having interconnect wiring therein sufficient for both operational testing and packaging of said semiconductor devices***...testing said devices via said wiring; and dividing said carrier into a plurality of components wherein each said component contains at least one said semiconductor device, as recited in independent claim 1, as amended.

Therefore, since the applied art does not teach or suggest all the claim limitations of independent claim 1, dependent claims 13-29 are also allowable.

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[7] *See* MPEP §2143.
[8] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.
[9] *In re Royka* 180 USPQ 580 (CCPA 1974).
[10] *In re Wilson*, 165 USPQ 494 (CCPA 1970) and *see MPEP* § 2143.03.
[11] *In re Ochiai*. 37 USPQ2d 1127 (Fed. Cir. 1995) and *see MPEP* § 2144.08.

Kaneko et al. Teaches Away, and Therefore is not Combinable

Further, it is impermissible within the framework of 35 U.S.C. §103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art.[12] Further in this regard, As the Court of Customs and Patent Appeals, predecessor to the Federal Circuit, has held:

> All relevant teachings of cited references must be considered in determining what they fairly teach to one having ordinary skill in the art. The relevant portions of a reference include not only those teachings which would suggest particular aspects of an invention to one having ordinary skill in the art, but also those teachings which would lead such a person away from the claimed invention.[13]

The rejections in the Official Action amount, in substance, to nothing more than hindsight reconstruction of Applicants' invention by relying on isolated teachings of the applied art, without considering the overall context within which those teachings are presented. Without benefit of Applicants' disclosure, a person having ordinary skill in the art would not know what portions of [Rostoker et al. and Kaneko et al.] to consider, and what portions to disregard as irrelevant or misleading.[14]

As discussed in the previous Response filed on February 11, 2003, Kaneko et al. is directed to a burn-in and test method of semiconductor wafers and burn-in boards for use in semiconductor burn-in tests which divides each semiconductor wafer into blocks which each include some integrated circuits, and which assigns each block an address to indicate in which part of the semiconductor wafer the integrated circuits of the block are placed.

These addresses in Kaneko et al. are recorded, and detachable carriers also having an identification code are loaded with a block to be tested. As discussed in Kaneko et al. (see col. 5, lines 7-13 when all the burn-in is finished, all carriers are removed from the burn-in board, and

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[12] *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 230 USPQ 416 (Fed. Cir. 1986).
[13] *In re Mercier*, 185 USPQ 774, 778 (CCPA 1975).
[14] *In re Wesslau*, 147 USPQ 391, 393 (CCPA 1965).

then, these carriers are fitted in the IC sockets of an IC tester for testing their characteristics. By handling and loading plural dies in block units, electrical connections to the burn-in and test apparatus are not as complicated, and the procedure is not a laborious as with so-called "die-by-die" loading.

Analysis of burn-in test results in Kaneko et al. permits the locating of defective integrated circuits in semiconductor wafers using the recorded addresses of the blocks, and the identification codes of the carriers. ***Once "good" chips are identified, they are removed from the carrier, and subsequently reattached to an operational carrier.***

That is, Kaneko et al. clearly teaches away from one aspect of the invention, by teaching that, after "good" chips are identified, they are removed from the carrier used in the burn-in test, and subsequently fitted into the IC sockets of an IC characteristics tester. Applicant presumes that subsequent removal from the IC tester and attachment to an end-use carrier follows a successful test of the IC characteristics.

Kaneko et al., therefore, represents a conventional, expensive and time-consuming temporary chip attachment, which is specifically disfavored by the approach of the present application, and which ***teaches away*** from at least one aspect of the invention claimed in independent claim 1.

Kaneko et al. represents an approach which is directly contrary to Applicants' recited limitation by not having ***interconnect wiring sufficient for both operational testing and packaging of the semiconductor devices.*** Kaneko et al. is therefore not properly combinable with Rostoker et al., even if relied upon for teaching limitations asserted by the Examiner to be unrelated to interconnect wiring or use both in operational testing and packaging of semiconductor devices.

Accordingly, reconsideration and allowance of claims 13-29 are requested.

Application No.: 09/588,617 Docket No.: 21806-00083-US

Allowable Subject Matter

Applicants note with appreciation the indication of allowable subject matter in dependent claims 6-12, but respectfully suggest that amendment of these claims into independent form is not necessary, in light of the allowability of independent claim 1, from which claims 6-12 depend.

Conclusion

In view of the above, each of the presently pending claims 1-32 in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner believes that an interview would serve to resolve any remaining issues in this application, the undersigned attorney is available at the telephone number indicated.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0456, under Order No. 21806-00083-US from which the undersigned is authorized to draw.

Respectfully submitted,

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BAA/LSH

Reply Due 2/14/04

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/588,617	06/06/2000	Claude L. Bertin	BUR9-1999-0264-US1	1077

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EXAMINER	
NGUYEN, TRUNG Q	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Abandonment	Application No.	Applicant(s)	
	09/588,617	BERTIN ET AL.	
	Examiner	Art Unit	
	Trung Q Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on 22 April 2003.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☒ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☒ The reason(s) below:

No reply has been received after 7 months. The Examiner called but no reply has been received.

KANAND CUED

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL

Search results for application number: 09/588,617			
Application Number:	09/588,617	Customer Number:	30678
Filing or 371(c) Date:	06-06-2000	Status:	Abandoned -- Failure to Respond to an Office Action
Application Type:	Utility	Status Date:	01-12-2004
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Group Art Unit:	2829	Location Date:	-
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Class/ Sub-Class:	324/765	Patent Number:	-
First Named Inventor:	Claude Bertin, South Burlington, VT	Issue Date of Patent:	-
Title Of Invention:	Carrier for test, burn-in, and first level packaging		

Foreign Priority | Continuity Data

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Number	Date	Contents Description
28	01-16-2004	File Marked Lost
27	01-14-2004	Mail Abandonment for Failure to Respond to Office Action
26	01-12-2004	Abandonment for Failure to Respond to Office Action
25	10-09-2003	Mail Notice of Restarted Response Period
24	10-08-2003	Letter Restarting Period for Response (i.e. Letter re: References)
23	08-14-2003	IFW TSS Processing by Tech Center Complete
22	04-22-2003	Mail Non-Final Rejection
21	04-21-2003	Non-Final Rejection
20	02-13-2003	Date Forwarded to Examiner
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18	11-20-2002	Mail Non-Final Rejection
17	11-18-2002	Non-Final Rejection
16	06-28-2002	New or Additional Drawing Filed
15	07-02-2002	Date Forwarded to Examiner
14	06-28-2002	Response after Non-Final Action
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12	03-28-2002	Mail Non-Final Rejection
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10	02-05-2002	Case Docketed to Examiner in GAU
9	11-06-2001	Case Docketed to Examiner in GAU
8	08-24-2000	Case Docketed to Examiner in GAU
7	07-21-2001	Case Docketed to Examiner in GAU
6	08-24-2000	Case Docketed to Examiner in GAU
5	06-06-2000	Information Disclosure Statement (IDS) Filed

4	08-15-2000	Application Dispatched from OIPE
3	08-15-2000	Correspondence Address Change
2	06-29-2000	IFW Scan & PACR Auto Security Review
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